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09/653,701	09/01/2000	Lorne Trottier	M1073-700719	5894

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EXAMINER	
ATALA, JAMIE JO	

ART UNIT	PAPER NUMBER
2621	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/653,701	TROTTIER ET AL.	
	Examiner	Art Unit	
	JAMIE JO VENT ATALA	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/6/09*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-7 and 9-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-7, 9-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed May 6, 2009 have been fully considered but they are not persuasive. Applicant argues that the declaration and exhibit provide detailed and comprehensive evidence of the reduction to practice; however, the examiner can not agree. As seen in Figure 4.1 (Exhibit B) the graphics accelerator chip (G400) has only one INPUT (Vin) and labeled video input. This input is the only input that provides "real-time uncompressed digital video streams" as recited in Claim 11. Furthermore, as seen in the marked up Figure of Exhibit B the graphics input (AGP) appears to be an output and does not serve as a second video input. The examiner notes that input is coming from the frame buffer; however, it is further noted that the frame buffer is not providing "uncompressed digital video streams". Therefore, the examiner does not feel the declaration and/or exhibit properly demonstrate "a graphics accelerator chip having at least two real-time uncompressed digital video streams.." as recited in Claim 11. Although, applicants points are understood the examiner can not agree and furthermore, since the prior non-final office action did not properly address the declaration and exhibit that rejection has been withdrawn and this office action will serve as a non-final office action. Furthermore, the examiner welcomes applicant to further explain Exhibit B in regards to the two inputs as discussed above regarding Claim 11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 3-7 and 9-32 are rejected under 35 U.S.C. 103(a) as being unpatentable by Frink et al (US 6,678,002) in view of MacInnis et al (US 6,853,385) in further view of Valmiki et al (US 2007/0217518).

[claim 11]

In regard to Claim 11, Frink et al discloses a video editing apparatus for performing video editing in real-time of video streams, the apparatus comprising:

- A video decoder for producing uncompressed digital video streams from said video streams (Figure 1a shows a HD codec 116 which decodes uncompressed digital video streams);
- A storage device for storing data (Figure 1a shows a HD disk buffer memory 114);
- A codec for providing at least two real-time uncompressed digital video streams from at least one of said video data provided by said storage device and said uncompressed digital video streams provided by said video decoder (Figure 1a shows HD codec 116 wherein the video streams from the storage device are uncompressed as discussed in Column 6 Lines 46+);

- A video encoder for providing a display signal from at least one of said uncompressed digital video streams and said edited uncompressed digital video streams (Figure 2 element 206 shows the input of the uncompressed data that is sent to the output 240);
- A first video bus for transferring said uncompressed digital video streams from said video decoder to said codec and for transferring said edited uncompressed digital video streams from said video output to said video encoder when said apparatus is operating in a real-time video editing mode (Figure 1a shows various buses transferring uncompressed digital video streams); and
- A time division multiplexed bus for transferring said at least two real-time uncompressed digital video streams from said codec to said at least two video inputs when said apparatus is operating in a real-time video editing mode (Figure 1f shows the various data buses as well as the buses being used to transfer data back to the codec during video capture mode); however fails to disclose
    - A graphics chip having at least two video inputs for respectively receiving said at least two real-time uncompressed digital video streams, said graphics chip further having a 2D graphics engine and a 3D rendering engine respectively for proving a 2D and 3D functions used for video editing of said at least two real-time uncompressed digital video streams, said graphics chip further

comprising a video output for providing edited uncompressed digital video streams:

MacInnis et al discloses a graphic processing system two video inputs receiving real time uncompressed video streams are entered into the graphics chip and a video output for providing uncompressed digital video streams as seen in Figure 1 and disclosed in Column 5 Lines 35+. Furthermore, the system has a 2D graphics engine and a 3D rendering engine for providing 2D and 3D function of the uncompressed digital video as disclosed in Column 60 Lines 1-30. The ability of the graphics processing circuit to generate both 2D and 3d images allows for a video system that has the ability to have various inputs to the system while rendering outputs of 2D and 3D video functions. Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use the graphic processing system, as disclosed by Frink et al, and further teach the system to have 2D and 3D function capability, as taught by MacInnis et al, to allow for efficient rendering of objects.

Valmiki et al further teaches a graphics accelerator chip having two uncompressed digital inputs as seen in Figure 1 and described in paragraphs 0083-0085. The graphic display system requires the two inputs for decoding and processing of the system to provide efficient display power to the user. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the he video editing apparatus, as disclosed by Frink et al in view of MacInnis, and further provide describe the graphic accelerator chip having two inputs, as described by Valmiki et al, to allow for a more efficient video editing system.

[claim 3]

In regard to Claim 3, Frink et al, discloses an apparatus wherein uncompressed digital video streams having been edited is transferred from said video output of the graphics processor to the codec for compression and storage in the video data storage device (Figure 2 shows the codec 216 which compresses the video signal from the router 220 and thereby gives an uncompressed or compressed video output to the storage device 102 as further described in Column 9 Lines 35).

[claim 4]

In regard to Claim 4, Frink et al, discloses an apparatus with a graphics chip with an input buffer for storing a sequence of fields of at least two real-time uncompressed digital video streams and an output buffer for storing a sequence of fields of said uncompressed digital video streams having been edited (Figure 1f shows the HD frame buffer 122, HD disk buffer memory 114 acts as input buffers to the graphics processor while the SDTV frame buffer acts as an output buffer for the output of the graphics processor).

[claim 5]

In regard to Claim 5, Frink et al, discloses an apparatus wherein the input buffer also stores input graphic image fields (Column 5 Lines 20-22 describe the input buffer and the storage of the graphic image fields).

[claim 6]

In regard to Claim 6, the claim limitations have been recited in Claim 4.

[claim 7]

In regard to Claim 7, the claim limitations have been recited in Claim 5.

[claim 9]

In regard to Claim 9, Frink et al, discloses an apparatus wherein the apparatus has an input for compressed digital video streams from an external device, and a decompression device, one of said at least two real-time uncompressed digital video streams comprising decompressed data from said compressed digital video stream (Figure 2 shows the input of the compressed digital video via element 240 and the decompression of the data in element 204 from the compressed signal).

[claim 10]

In regard to Claim 10, Frink et al, fails to disclose the input for compressed digital video streams comprises one of an IEEE 1394 interface and an SDTI interface.

The examiner takes official notice that it is well known in the art that compressed digital video input can have various interfaces including IEEE 1394 and SDTI. It would have been obvious to one skilled in the art at the time of the invention to incorporate these interfaces into data communication aspect of the invention disclosed by Frink et al.

[claim 12]

In regard to Claim 12, Frink et al discloses an apparatus wherein the video decoder uses said first video bus for transferring uncompressed video digital video streams to said video encoder in a non-editing playback mode and said video decoder uses said first video bus for transferring uncompressed digital video streams from said video decoder to said codec in a video capture mode (Figure 1f shows the various data buses

as well as the buses being used to transfer data back to the codec during video capture mode).

[claim 13]

In regard to Claim 13, Frink et al discloses an apparatus for input of compressed digital video streams wherein each of at least two video input is coupled to said 3D and 2D rendering engine, and wherein said video output is coupled to said 3D and 2D engines. MacInnis et al discloses a system has a 2D graphics engine and a 3D rendering engine for providing 2D and 3D function of the uncompressed digital video as disclosed in Column 60 Lines 1-30. The ability of the graphics processing circuit to generate both 2D and 3d images allows for a video system that has the ability to have various inputs to the system while rendering outputs of 2D and 3D video functions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the video editing apparatus, as disclosed by Frink et al, and incorporate a system wherein a graphics chip ability to render 2D and 3D images are able to handle the functions for display, as disclosed in MacInnis et al.

[claim 14]

In regard to Claim 14, the claim limitations have been recited in Claim 13.

[claim 15]

In regard to Claim 15, the claim limitations have been recited in Claim 11

[claim 16]

In regard to Claim 16, Frink et al discloses a system; however fails to disclose an act of mapping at least one of the first real-time uncompressed digital video stream and the

second real-time uncompressed digital video stream onto a target surface and a buffer included in the graphics chip and the first time uncompressed digital video stream originates from a video storage medium.

MacInnis discloses a system wherein first and second real-time uncompressed digital video stream provides a target surface wherein the information is processed into a buffer as described in Column 5 Lines 35+ through Column 2 Lines 1-30. Furthermore, as seen in Figure 1 the graphics chip has various inputs and described in Column 5 Lines 35-45 the inputs can ranges from various inputs including information that has been stored on a medium. The system has the capability to have various inputs to allow for the system to handle and process the various inputs with efficiency. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the system as disclosed by Frink et al, and incorporate a system that allows various inputs into the graphics chip, as recited by MacInnis et al.

[claim 17]

In regard to Claim 17, the claim limitations have been recited in Claim 16.

[claim 18]

In regard to Claim 18, the claim limitations have been recited in Claim 16.

[claim 19]

In regard to Claim 19, the claim limitations have been recited in Claim 16.

[claim 20]

In regard to Claim 20, the claim limitations have been recited in Claim 16.

[claim 21]

In regard to Claim 21, the claim limitations have been recited in Claim 16.

[claim 22]

In regard to Claim 22, the claim limitations have been recited in Claim 11.

[claim 23]

In regard to Claim 23, the claim limitations have been recited in Claim 11.

[claim 24]

In regard to Claim 24, the claim limitations have been recited in Claim 11.

[claim 25]

In regard to Claim 25, Frink et al discloses an apparatus as claimed in claim 24, further comprising a codec and a storage device, wherein uncompressed digital video streams having been edited are transferred from said video output of said graphics accelerator chip to said codec for compression and storage in said storage device (Figure 5 shows the compression that is done after the input signals are processed).

[claim 26]

In regard to Claim 26, the claim limitations have been recited in Claim 4.

[claim 27]

In regard to Claim 27, the claim limitations have been recited in Claim 5.

[claim 28]

In regard to Claim 28, the claim limitations have been recited in Claim 9.

[claim 29]

In regard to Claim 29, the claim limitations have been recited in Claim 10.

[claim 30]

In regard to Claim 30, the claim limitations have been recited in Claim 11.

[claim 31]

In regard to Claim 31, MacInnis et al teaches a graphic accelerator chip further includes a first buffer coupled to the first input wherein the first input is coupled to the 2D graphics engine and the 3D rendering engine via the first input buffer and a second input buffer couples to the second video input wherein the second video input is coupled to the 2D graphics engine and 3D rendering engine via the second input buffer (The system has a 2D graphics engine and a 3D rendering engine for providing 2D and 3D function of the uncompressed digital video as disclosed in Column 60 Lines 1-30).

[claim 32]

In regard to Claim 32, MacInnis et al teaches a graphics accelerator chip including a graphics input buffer couple to the graphics unit wherein the graphics input is coupled to the 2D graphics engine and the 3D rendering engine via the graphics input buffer (Column 60 Lines 1-30 describe the input to the 2D graphics engine).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Trottier et al (US 6,763,176)

Jain et al (US 5,745,126).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE JO VENT ATALA whose telephone number is (571)272-7384. The examiner can normally be reached on 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran can be reached on 571-272-7382. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/JAMIE JO VENT ATALA/
Examiner, Art Unit 2621